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Masleid

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(54) **POWER EFFICIENT MULTIPLEXER**

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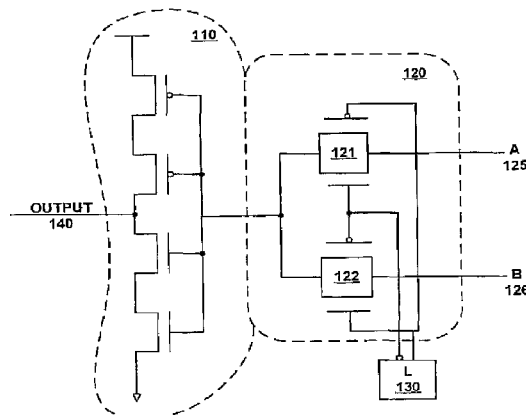
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(57) **ABSTRACT**

A power efficient multiplexer. In accordance with a first embodiment, a power efficient multiplexer comprises a transmission gate structure for selectively passing one of a plurality of input signals and a stacked inverter circuit for inverting the one of a plurality of input signals. Both the stacked inverter and the transmission gate provide beneficial reductions in static power consumption in comparison to conventional multiplexer designs.

15 Claims, 4 Drawing Sheets

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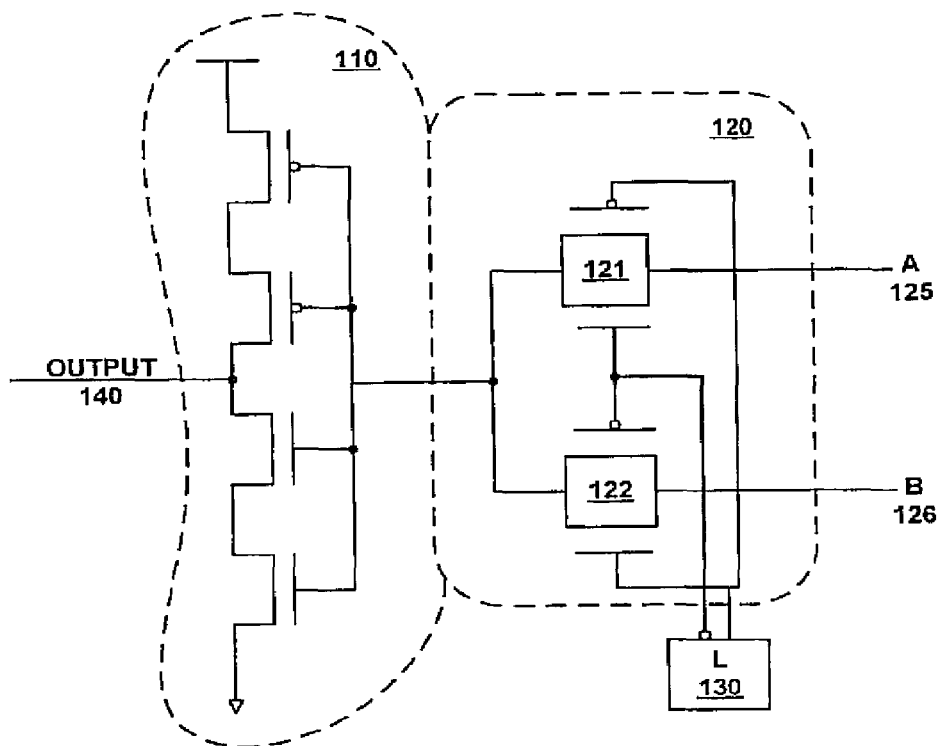
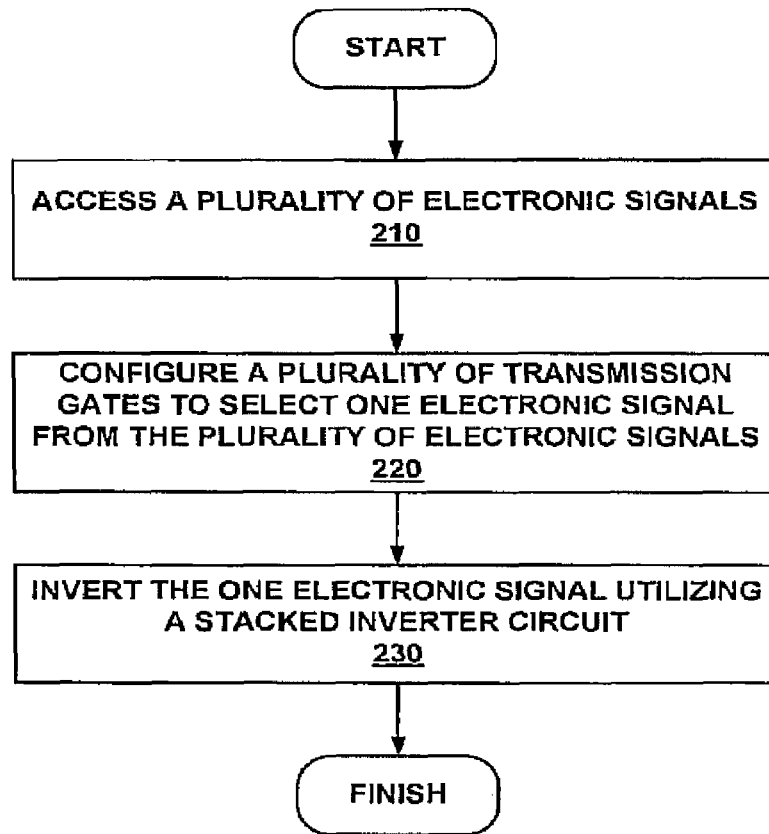Rhyne, "Fundamentals of Digital Systems Design", N.J., Jan. 1973, pp. 70-71.

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FIGURE 1

200

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                    ┌─────────────┐
                    │    START    │
                    └──────┬──────┘
                           │
                           ▼
        ┌──────────────────────────────────────────┐
        │  ACCESS A PLURALITY OF ELECTRONIC SIGNALS │
        │                   210                      │
        └──────────────────┬───────────────────────┘
                           │
                           ▼
        ┌──────────────────────────────────────────┐
        │  CONFIGURE A PLURALITY OF TRANSMISSION    │
        │  GATES TO SELECT ONE ELECTRONIC SIGNAL    │
        │  FROM THE PLURALITY OF ELECTRONIC SIGNALS │
        │                   220                      │
        └──────────────────┬───────────────────────┘
                           │
                           ▼
        ┌──────────────────────────────────────────┐
        │  INVERT THE ONE ELECTRONIC SIGNAL UTILIZING│
        │        A STACKED INVERTER CIRCUIT          │
        │                   230                      │
        └──────────────────┬───────────────────────┘
                           │
                           ▼
                    ┌─────────────┐
                    │   FINISH    │
                    └─────────────┘
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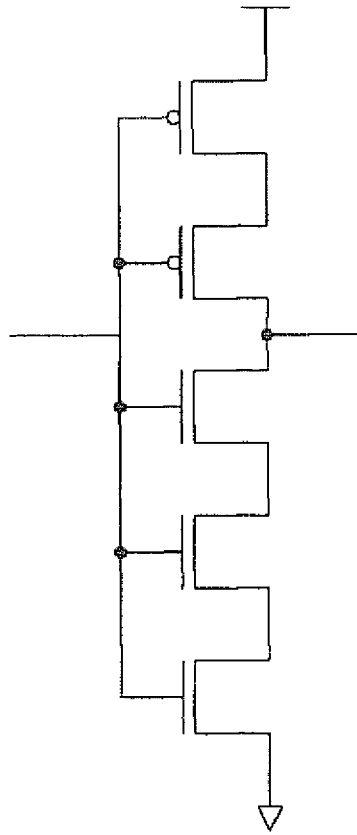
FIGURE 2

FIGURE   3

FIGURE   4

POWER EFFICIENT MULTIPLEXER

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a Continuation of and claims priority to U.S. patent application Ser. No. 13/356,396, filed on Jan. 23, 2012, which is a Continuation of and claims priority to U.S. patent application Ser. No. 12/397,085, filed on Mar. 3, 2009, and now issued as U.S. Pat. No. 8,102,190, which is a Continuation of and claims priority to U.S. patent application Ser. No. 11/021,632, filed on Dec. 23, 2004, and now issued as U.S. Pat. No. 7,498,846, which is a Continuation-In-Part of and claims priority to U.S. patent application Ser. No. 10/864,271, filed on Jun. 8, 2004, and now issued as U.S. Pat. No. 7,336,103, which are hereby incorporated by reference in their entirety.

This application is related to the following commonly assigned United States patent applications, which are hereby incorporated herein by reference in their entirety:

U.S. patent application Ser. No. 11/021,222, filed Dec. 23, 2004, now U.S. Pat. No. 7,635,992, entitled "A Configurable Tapered Delay Chain with Multiple Sizes of Delay Elements" by Masleid;

U.S. patent application Ser. No. 11/021,221, filed Dec. 23, 2004, now U.S. Pat. No. 7,656,212, entitled "A Configurable Delay Chain with Switching Control for Tail Delay Elements" by Masleid;

U.S. patent application Ser. No. 11/021,197, filed Dec. 23, 2004, now U.S. Pat. No. 7,332,931, entitled "Leakage Efficient Anti-glitch Filter with Variable Delay Stages" by Masleid;

U.S. patent application Ser. No. 11/020,746, filed Dec. 23, 2004, now U.S. Pat. No. 7,310,008, entitled "A Configurable Delay Chain with Stacked Inverter Delay Elements" by Masleid; and

U.S. patent application Ser. No. 11/021,633, filed Dec. 23, 2004, now U.S. Pat. No. 7,330,054, entitled "Leakage Efficient Anti-glitch Filter" by Masleid.

FIELD

Embodiments relate to power efficient multiplexers.

BACKGROUND

Static power consumption in modern semiconductor processes, e.g., processes with a minimum feature size of about 0.13 microns and smaller, is no longer a negligible component of total power consumption. For such processes, static power may be one-half of total power consumption. Further, static power, as a percentage of total power, is tending to increase with successive generations of semiconductor process. Consequently, circuit elements that are efficient in terms of static power consumption are highly desired. One commonly utilized circuit element is a multiplexer. In general, a multiplexer selects among several inputs to propagate to its output. For example, variable delay circuits generally require a series of multiplexers to select between a signal present at a desired tap of the delay circuit and a signal propagating from beyond a desired tap.

SUMMARY

A power efficient multiplexer is disclosed. In accordance with a first embodiment, a power efficient multiplexer comprises a transmission gate structure for selectively passing

one of a plurality of input signals and a stacked inverter circuit for inverting the one of a plurality of input signals.

In accordance with another embodiment, the plurality of electronic signals is accessed. A method of selecting one electronic signal from a plurality of electronic signals is disclosed. A plurality of transmission gates is configured to select one electronic signal from the plurality of electronic signals. The one electronic signal is inverted utilizing a stacked inverter circuit

In accordance with still another embodiment, an electronic circuit comprises a stacked inverter circuit. The stacked inverter circuit comprises at least two devices of a first type coupled in series. These devices are coupled in series to a group of at least two devices of an opposite type coupled in series. The electronic circuit further comprises a first conductance terminal of a first transmission gate coupled to a first electronic signal and a first conductance terminal of a second transmission gate coupled to a second electronic signal. The second conductance terminals of the first and second transmission gates are coupled to an input of the stacked inverter circuit. The first control terminal of a semiconductor type of the first transmission gate is coupled to a second control terminal of opposite semiconductor type of the second transmission gate. The second control terminal of the opposite semiconductor type of the first transmission gate is coupled to a first control terminal of the semiconductor type of the second transmission gate.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments, together with the description, serve to explain the principles of the disclosure.

FIG. 1 illustrates a schematic of a novel power efficient multiplexer, in accordance with embodiments.

FIG. 2 illustrates a flow chart for a method 200 of selecting one electronic signal from a plurality of electronic signals, in accordance with embodiments.

FIG. 3 and FIG. 4 illustrate it is possible to stack different numbers of transistors on either or both legs of a stacked inverter in accordance with embodiments.

DETAILED DESCRIPTION

Reference will now be made in detail to embodiments, examples of which are illustrated in the accompanying drawings. While the disclosure will be described in conjunction with these embodiments, it will be understood that they are not intended to limit the disclosure to these embodiments. On the contrary, the disclosure is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the disclosure as defined by the appended claims. Furthermore, in the following detailed description, numerous specific details are set forth in order to provide a thorough understanding. However, it will be recognized by one of ordinary skill in the art that embodiments may be practiced without these specific details.

Power Efficient Multiplexer

Embodiments are described in the context of design and operation of integrated semiconductors. More particularly, embodiments relate to power efficient multiplexers. It is appreciated, however, that embodiments may be utilized in other areas of semiconductor design and operation.

The following description of embodiments is directed toward pFETs (or p-type metal oxide semiconductor field effect transistors (MOSFETS)) formed in surface N-wells

and/or nFETs (or n-type MOSFETS) formed in surface P-wells when a p-type substrate and an N-well process are utilized. It is to be appreciated, however, that embodiments are equally applicable to nFETs (or n-type MOSFETS) formed in surface P-wells and/or pFETs (or p-type MOS-FETS) formed in surface N-wells when an n-type substrate and a P-well process are utilized. Consequently, embodiments are well suited to semiconductors formed in both p-type and n-type materials, and such embodiments are considered within the scope of the disclosure.

FIG. 1 illustrates a schematic of a novel power efficient multiplexer **100**, in accordance with embodiments. Power efficient multiplexer **100** comprises an inverter **110** and a transmission gate structure **120**. Transmission gate structure **120** comprises transmission gates **121** and **122**.

A bit value in latch **130** determines whether transmission gate **121** is "open" or "closed," for example whether transmission gate **121** passes a signal or not. Similarly, the bit value in latch **130** determines whether transmission gate **122** passes a signal or not. Both transmission gates **121** and **122** are controlled by the same bit value and that bit value's complement. Consequently, either transmission gate **122** will pass a signal, or transmission gate **121** will pass a signal, but not both simultaneously.

For example, in the embodiment of FIG. **1**, a zero value in latch **130** will cause transmission gate **121** to pass signal A **125**, while causing transmission gate **122** not to pass any signals. Consequently, transmission gate structure **120** will select signal A **125** corresponding to a zero value in latch **130**.

Similarly, a one value in latch **130** will cause transmission gate **122** to pass signal B **126**, while causing transmission gate **121** not to pass any signals. Consequently, transmission gate structure **120** will select signal B **126** corresponding to a one value in latch **130**.

The signal, A **125** or B **126**, selected by transmission gate structure **120** is inverted by inverter **110** to produce output **140** of power efficient multiplexer **100**.

It is to be appreciated that static power consumption in modern semiconductor processes, e.g., processes with a minimum feature size of about 0.13 microns and smaller, is no longer a negligible component of total power consumption. For such processes, static power may be one-half of total power consumption. Further, static power, as a percentage of total power, is tending to increase with successive generations of semiconductor process.

Advantageously, inverter **110** comprises stacked field effect transistors (FETs). In general, an inverter stage, whether conventional or stacked, forms a leakage path, e.g., a series "string" of devices coupled from operating voltage (Vdd) to ground. As current leaks through such leakage paths, static power is consumed by the inverter stage. As described more completely in U.S. patent application Ser. No. 10/864, 271, entitled "Stacked Inverter Delay Chain" to Masleid and Burr, incorporated herein by reference in its entirety, an inverter comprising stacked field effect transistors can consume less static power than a conventional inverter to produce a comparable delay.

Further, such leakage paths within a stacked inverter suffer less leakage than a conventional inverter, yielding additional beneficial leakage reductions. In a conventional inverter, exactly one transistor is on while the other transistor is off. As an unfortunate consequence, approximately the full bias voltage is applied to the off transistor, resulting in a maximum possible leakage for the off transistor.

In contrast, in a stacked inverter multiple transistors are either on or off in series. For example, in the embodiment of FIG. **1**, for a "high" state, two transistors are on, while two

transistors are off. Consequently, each "off" transistor has significantly less than full bias voltage applied. It is appreciated that leakage current generally decreases exponentially as voltage decreases. For example, a factor of two reduction in off bias voltage produces about a factor of eight reduction in leakage current per leakage path.

It is to be further appreciated that such leakage induces non zero voltages at intermediate nodes between the off transistors. Such voltages induce body effects in the transistors. Such body effects increase the threshold voltage of the affected transistors. An increased threshold voltage generally produces beneficial decreases in leakage current.

Consequently, in addition to a decrease in a number of leakage paths, in accordance with embodiments, the leakage current of each path is very beneficially reduced due to an induced body effect and a highly non-linear relationship between bias voltage and leakage current. Thus, inverter **110** significantly reduces static power consumption, in comparison to a conventional inverter.

It is to be appreciated that more or fewer stacked FETs can be can be included in inverter **110** in order to achieve differing signal propagation and/or power characteristics, in accordance with embodiments.

For example, physical differences between electrons and holes, and between n-type and p-type dopants, as well as constructive differences in device geometry and dopant placement, result in differences in efficiency between n-type devices and p-type devices. Because electron mobility is higher than hole mobility, n-type devices are more efficient than p-type devices. However, the degree of difference depends on constructive differences that can vary with process. Such physical and constructive differences also produce other behavior differences, such as a difference in sensitivity to body effects. Consequently, different levels of benefit, e.g., in leakage reduction, are to be expected between stacks of n-type devices and stacks of p-type devices. To allow for such effects, in accordance with embodiments, it is possible to stack different numbers of transistors on either or both legs of a stacked inverter (e.g., FIG. **3** and FIG. **4**). Such variations allow increases in load and/or decreases in drive capability, enabling a wide variety of loading and drive characteristics, as well as enabling differing body effects.

Also of benefit in reducing power consumption, particularly static power consumption, of power efficient multiplexer **100** is transmission gate structure **120**. It is to be appreciated that transmission gates, for example transmission gates **121** and **122**, are characterized as having no direct path between power (Vdd) and ground. Consequently, transmission gates are characterized as having extremely small leakage, and thus very little static power consumption.

It is appreciated that a variety of factors, e.g., operating voltage, operating temperature and/or manufacturing process variations, can affect the speed of operation of an integrated circuit. It is generally desirable for a multiplexer to track speed changes of other circuitry of an integrated circuit. For example, if other circuits of an integrated circuit operate faster, generally a multiplexer is required to select a desired signal more quickly in order for the overall circuit to function. Because embodiments comprise stacked devices, they are similar to many logic circuits that also comprise stacked devices, e.g., NAND and/or NOR logic gates. Consequently, embodiments match or track changes in operating speed of complex logic more accurately than multiplexers comprising very simple inverters.

It is to be appreciated that embodiments are well suited to selecting among more than the two signals illustrated in FIG.

1, and embodiments comprising more than two selectable signals are to be considered within the scope of the disclosure.

Embodiments are thus shown to offer significant and highly beneficial improvements in tracking timing changes of other circuits and in static power (leakage current) consumption in comparison to the conventional art.

FIG. 2 illustrates a flow chart for a method **200** of selecting one electronic signal from a plurality of electronic signals, in accordance with embodiments. In **210**, the plurality of electronic signals is accessed. For example, referring to FIG. **1**, the plurality of electronic signals is accessed at transmission gates **121** and **122**.

In **220**, a plurality of transmission gates is configured to select one electronic signal from the plurality of electronic signals. For example, referring to FIG. **1**, a zero value in latch **130** will cause transmission gate **121** to pass signal A **125**, while causing transmission gate **122** not to pass any signals. Consequently, transmission gate structure **120** will select signal A **125** corresponding to a zero value in latch **130**.

In **230**, the one electronic signal is inverted utilizing a stacked inverter circuit, for example stacked inverter circuit **110** of FIG. **1**.

The foregoing descriptions of specific embodiments have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the disclosure to the precise forms disclosed, and many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the disclosure and its practical application, to thereby enable others skilled in the art to best utilize the disclosure and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the disclosure be defined by the Claims appended hereto and their equivalents.

What is claimed is:

1. A method comprising:

outputting, from a latch circuit, at least one bit and a complement of the at least one bit;

selectively passing one of a plurality of input signals by using the at least one bit and the complement; and

independently of the at least one bit and the complement and a state of a clock signal, inverting an input signal from said selectively passing, wherein said inverting includes:

using a stacked inverter to invert the input signal from said selectively passing, wherein the stacked inverter comprises a low-to-high transition leg that includes a first number of transistors and a high-to-low transition leg that includes a second number of transistors that is different relative to the first number of transistors.

2. The method of claim **1**, wherein said selectively passing comprises:

applying the at least one bit to a first transmission gate and a second transmission gate; and

applying the complement to the first transmission gate and the second transmission gate.

3. The method of claim **2**, wherein said selectively passing further comprises:

if the at least one bit is a first value, outputting a first input signal from the first transmission gate.

4. The method of claim **3**, wherein said selectively passing further comprises:

if the at least one bit is a second value, outputting a second input signal from the second transmission gate.

5. The method of claim **1**, wherein the first number is greater than the second number.

6. The method of claim **1**, wherein the first number is less than the second number.

7. A method comprising:

outputting, from a latch circuit, at least one bit and a complement of the at least one bit;

if the at least one bit is a first value, passing a first input signal by using the at least one bit and the complement;

if the at least one bit is a second value, passing a second input signal by using the at least one bit and the complement; and

independently of the at least one bit and the complement and a state of a clock signal, inverting an input signal from at least one of said passing a first input signal or said passing a second input signal, wherein said inverting includes:

using a stacked inverter to invert the input signal from at least one of said passing a first input signal or said passing a second input signal, wherein the stacked inverter comprises a low-to-high transition leg that includes a first number of transistors and a high-to-low transition leg that includes a second number of transistors that is different relative to the first number of transistors.

8. The method of claim **7**, further comprising:

applying the at least one bit to a first transmission gate and a second transmission gate; and

applying the complement to the first transmission gate and the second transmission gate.

9. The method of claim **8**, wherein said passing a first input signal comprises:

outputting the first input signal from the first transmission gate.

10. The method of claim **8**, wherein said passing a second input signal comprises:

outputting the second input signal from the second transmission gate.

11. The method of claim **7**, wherein the first number is greater than the second number.

12. The method of claim **7**, wherein the first number is less than the second number.

13. A method comprising:

accessing a plurality of input signals;

outputting, from a latch circuit, at least one bit and a complement of the at least one bit;

using the at least one bit and the complement to select one of the plurality of input signals; and

independently of the at least one bit and the complement and a state of a clock signal, inverting an input signal from said using, wherein said inverting includes:

utilizing a stacked inverter to invert the input signal from said using, wherein the stacked inverter comprises a low-to-high transition leg that includes a first number of transistors and a high-to-low transition leg that includes a second number of transistors that is different relative to the first number of transistors.

14. The method of claim **13**, wherein the first number is greater than the second number.

15. The method of claim **13**, wherein the first number is less than the second number.

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